"Towards Global Technological Excellence"
GOVERNMENT COLLEGE OF ENGINEERING, AMRAVATI
(*An Autonomous Institute of Government of Maharashtra*)
Near Kathora Naka, Amravati, (M. S.), India, Pin: 444 604

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No. GCoEA/E&Tc/Quotation/2024-25/ 3753
Date: 06/08/2024

To,
m/s ----------
----------List is attached herewith----------

Subject: - Quotation for the Hands-on training on **"Next-Generation Nano-Electronic Devices, Circuits and its Applications using EDA Simulation tools"** in the Department of Electronics Engineering at **Government College of Engineering, Amravati**.

Dear Sir,
Hereby quotations with lowest reasonable rates for the following training content are being called; send your quotation in the sealed cover to reach the undersigned on or before 14/08/2024.

Sr. No.	Content	Details
1.	**Training Title**	Hands-on training on "**Next-Generation Nano-Electronic Devices, Circuits and its Applications using EDA Simulation tools**"
2.	**Training Venue**	College premises
3.	**Training Duration**	03 days
4.	**Training Material**	Training Material must be handover to the participants on the commencement of the training
5.	**Training Certificate**	Certificate for all the participants
6.	**Licensed software tools during training session**	a. Training must be provided with the Licensed EDA software tools. b. Licensed software must be for all participants on their personal machines/laptops. c. Licensed software provided must be valid for 3 Months from the date of training. d. PLD Hardware must be provided for the group of students during training duration.

7.	**Training Objectives**	a. Exposure to VLSI/ ASIC Design b. Hands on VLSI Back end design tools c. Hands on VLSI Front end design tools d. To study the CMOS VLSI Design Issues e. Hands-on with the FPGA PLD platform
8.	**Training Syllabus**	• Introduction to CMOS VLSI and ASIC Design Flow • Introduction to PLD platforms • Mixed Signal Simulation using SPICE netlist • Introduction to FinFET technology • FinFET design and analysis • Nano-sheets (NSFETs) based design and analysis • CMOS Inverters: DC & Transient Response • Transistor sizing, W/L calculations, Lambda parameter • Combinational & Sequential CMOS Design • Design rule check with Technology Scaling • Power, I/O and Clock Design • Signal Integrity Issues • Case Study
9.	**Target Participant**	Final Year B. Tech. (min. 60 Seats)
10.	**Detailed Training contents must be:**	**Recent trends in VLSI Technology, Current VLSI industries Scenario** **Front End & Back End**, Introduction to CMOS VLSI design and basics design techniques, Fabrication Techniques. **Ultra-Deep-Submicron CMOS** cell design issues, introduction to planar nanometer technologies, strained silicon design, design rules & characteristics, ASIC design flow, techniques for improving power consumption and speed, backend design issues & applications. **Design with FinFET 14/10/7 nm technology nodes.** • Introduction and design trends with NSFETs. • EDA software & illustration of design techniques Overview of practical • Designing and analysis of basics of NMOS and PMOS transistors, Strong and Weak concept of transistor and Illustration of why we prefer CMOS technology. • ASIC design flow and design styles, Full custom and Semi-custom Design of CMOS Inverter with Hands on session, W/L ratio and its importance. Sizing factor, Concept: Mobility principle, Electro-migration principle • Designing of universal gates and Analysis. Practical session using schematic & layout Practical concepts, and experimentation

		• Assignment Session - Complex Inverter design with huge load. Hands – on session. • CMOS Circuit Design & Analysis • Transistorized layout designing • Design of basic CMOS circuits and their analysis techniques. Requirement identification and result calculation, identifying the list of experiments. • Design of CMOS circuits using stick diagrams; like basic gates, current mirror, etc. • Practical session using schematic & layout Practical concepts, and experimentation. • Digital CMOS circuit design and optimization • Input variations **Module level design approach** • Assignments Session- Difference between 2:1 MUX by logic gates and transmission gate • Assignments on Digital CMOS circuit design and optimization • Designing of Oscillators • Layout optimization using netlist for ASIC **Mixed Signal Simulation** • The design of basic logic gates introducing interconnect design, compact design strategies, and impact on switching speed and power consumption. • The design of analog blocks introducing amplification, voltage reference, addition of analog signals, and mixed-signal blocks. • Hands on session using SPICE netlist simulation software tools **Digital CMOS circuit design and optimization** • Assignments on Digital CMOS circuit design and optimization • Assignments on Optimal Analog CMOS circuit design. • Practical session using schematic & layout Practical concepts, and experimentation • CMOS Differential Amplifire and its analysis. • Analysis with CMRR (Ad and Acm), Output impedance, Bandwidth • Layout optimization using netlist for ASIC. **Analog VLSI Design** • The design of analog VLSI design with interconnect design, compact design strategies, and impact on

		switching speed and power consumption. The design of analog blocks introducing amplification, voltage reference, addition of analog signals, and mixed-signal blocks. **Circuit Characterization and Performance Estimation** • Resistance and capacitance estimation, switching characteristics, power dissipation, charge sharing. • Hands on session • Design of Analog circuits using stick diagrams; like basic gates, current mirror, etc. • CMOS circuit design and optimization • Assignments on Optimal Analog CMOS circuit design. • Sample and hold circuit • Layout designing and analysis of higher end examples • Comparator, ADC and DAC using CMOS circuits, case study of Phase Lock Loop design. • CMOS Current Mirror circuit design and analysis Introduction to FinFET and NSFET technology • Designing of FinFET 14 nm with Hands on session • Circuit Characterization and Performance Estimation • Resistance and capacitance estimation, switching characteristics, power dissipation, charge sharing. • Schimitt Trigger and its analysis UTP and LTP Value finding • Designing of VCO

Note:

- The dispatch number of this office i.e. outward number of the quotation call letter, the name of the department for which the quotation is desired and the heading "Quotation for the training of _____", should necessarily be superscribed on the main envelope.

TERMS & CONDITIONS

It is proposed to have a Two Envelops System for this Quotation: Envelops should be sealed with a mention of the type of envelop (Technical / Financial) and the outward number of the quotation call letter. These two envelops should be sealed in a third (main) envelop, as mentioned above.

Technical Specifications – Cover should contain Technical specifications document.

A) **Covering letter** for the quotation on the letter head of the supplier.
B) **Establishment certificate** must be enclosed.
C) ST/CST/VAT/**GST registration certificate** along with respective **clearance certificate** for the assessment year is also necessary.

D) **No-Deviation Statement:** No-Deviation statement for specification of the Training offered giving details of specifications in following pro-forma only (No other format will be accepted).

Supplier must fill the specified pro-forma and mere certifying that 'There is no deviation between Enquiry specifications and specifications quoted by the bidder' is not acceptable and such quotations are likely to be rejected.

E) **Purchase order of the previously deployed training must be submitted with the proposal**

(2) **Commercial Quotation** – Cover should contain price quote document.

A) **Validity:** The rates offered should be valid till 31/03/2025.

B) **Price:** F.O.R. destination at Government College of Engineering, Amravati. The offer should be firm, inclusive of all taxes. No extra charges will be paid. If needed, taxes, duties, charges etc. should be clearly mentioned.

C) **Payment: 100%** against satisfactory completion of training.

D) **Training material** should be supplied at the time of training free of cost.

E) The undersigned reserves the right to accept or reject any offer or all offers without assigning any reason thereof.

F) The undersigned shall not incur any liability to pay interest for delay in payment of bills for any reasons what so ever.

Government College of Engineering Amravati

Principal
Government College of Engineering, Amravati

Proforma of No-Deviation Certificate

Name of the Supplier:

Specification of Training stated in Enquiry step by step as per specifications mentioned in document	Specification of Training offered by the supplier step by step	Whether there are deviation from the tender specification, Yes / No	If yes, indicate clearly which the deviations are
1	2	3	4
Specification detail1 1,			
Specification detail 2…			
etc.			

Signature of Supplier with Seal